REMARKS/ARGUMENTS

Claim Rejections – 35 USC § 103. The Office Action rejected claims 1-17 under Section 103(a) as being unpatentable over Datar et al. (U.S. 6,625,740) in view of Ellenby et al. (U.S. 6,064,398) or Dendinger (U.S. 6,714,891. The Office Action rejected claims 1-17 under Section 103(a) as being unpatentable over Miller (US 2002/0144030) in view of Ellenby et al. or Dendinger. Thus, the Datar et al., Ellenby et al., Dendinger and Miller patents have been cited to reject the pending patent claims. The Applicant respectfully traverses the rejections for the following reasons.

Prima facie obviousness is established only if the Examiner shows that (1) there is some teaching, suggestion, or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference; (2) there is a reasonable expectation of success; and (3) the prior art teaches or suggests all of the claim elements. *MPEP* § 2143.03. Applicants respectfully assert that the Examiner has not established *prima facie* obviousness of the rejected claims.

In the present case, none of the cited references disclose or suggest that the image data is directly written into the AGP memory block of the system memory instead of the non-AGP memory block of the system memory, as recited in the amended claim 1. Similarly, none of the cited references disclose or suggest that the received data is written into a specified memory block of said system memory, which is accessible by said graphics accelerator, without transference of the image data inside the system memory, as recited in the amended claim 9 or 11. Given that the cited prior art fails to teach or suggest all of the recited claim elements, the Examiner has not established *prima facie* obviousness of the rejected claims. Withdrawal of the rejections and allowance of the pending claims is respectfully requested.

Datar et al. The Datar et al. patent discloses systems and methods for saving power on an integrated circuit. Datar et al.'s Figure 1 discloses a graphics accelerator 107, an AGP bus 106, north bridge 103, and system memory 102, similar to Figure 1 of the present specification. Datar does not disclose or suggest an AGP memory block and a non-AGP memory block. The Office Action (paragraphs 2 and 3) falsely states that Datar teaches system memory "having an AGP memory block and a non-AGP memory block," because there is no such disclosure by Datar.

Datar fails to disclose or suggest "writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block."

Paragraph 2 of the Office Action acknowledges that Data fails to disclose the claimed step of "writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block," but argues that this step is "inherent" because Datar discloses an AGP bus. According to the Examiner, one reason to use an AGP bus "is for the graphics accelerator to ***directly access*** [a] portion of the system memory." Directly accessing a portion of memory is not equivalent to ***directly writing*** to an AGP memory block in system memory. The rejected claims plainly differentiate between ***accessing*** system memory and ***writing*** to system memory. Applicant does not question that the use of the AGP bus permits the graphics accelerator to ***directly access*** the AGP memory block; however, there is no teaching, suggestion, motivation, or support for the Examiner's assumption that the existence of an AGP bus inherently discloses ***directly writing*** to the AGP memory block as claimed. Obviousness under Section 103 cannot be established by an unsupported "inherent" disclosure or assumption.

Ellenby et al. The Ellenby et al. patent is directed to an image processing system for producing an augmented image of a real world scene that uses an image capturing device that captures a digital image of the real world scene and uses a database of real world scene information to augment the image. Ellenby's Fig. 2 discloses a 3D graphics processor 116 with a PCI interface. Ellenby does not disclose an AGP bus or an AGP memory block. Ellenby discloses a digital camera connected to a firewire video interface chipset 104. The Ellenby patent was cited by the Examiner because it states at column 6, lines 17-20: "Chipset 104 can also operate as a PCI Bus Master, thus can burst image data to anywhere in the CPU's main memory or to any PCI slave device's memory." Because Ellenby does not disclose an AGP memory block, Ellenby plainly fails to disclose or suggest "writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block."

Dendinger. The Dendinger patent discloses a method and apparatus for thermal management of a power supply to a computer processor. A sensor monitors the temperature of the power supply that delivers chip core current to a computer processor. A reduction in, but not compete stoppage of, the performance of the data processor is requested in response to the

temperature having risen to a predetermined threshold. Dendinger discloses a peripheral device, such as a digital camera, may be connected to a USB controller. The ability to connect a digital device, such as a camera, to a computer via a USB controller has nothing to do with the present invention. Dendinger plainly fails to disclose or suggest "writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block."

Miller. The Miller publication discloses an apparatus and method for loading and enabling firmware software support for an input device coupled to an electronic device if a switch is pressed and held for a predetermined period of time at a time when the electronic device is turned off. Miller's Fig. 1 discloses an AGP slot 140 for a graphics board (not shown) coupled to a north bridge IC 120. Fig. 1 also discloses memory slots 130 for SIMM or DIMM sockets. Miller does not disclose or suggest an AGP memory block and a non-AGP memory block. The Office Action (paragraphs 4 and 5) falsely states that Miller teaches system memory "having an AGP memory block and a non-AGP memory block," because there is no such disclosure by Miller. Miller fails to disclose or suggest "writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block."

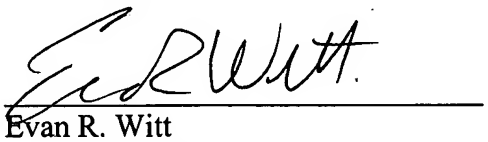
For the same reasons as with the Datar patent discussed above, the Office Action argued because Miller allegedly discloses an AGP bus that Miller inherently disclosed directly writing image data into the AGP memory block. This assumption and logic is erroneous for the same reasons given above.

Because neither Datar, Miller, Ellenby, nor Dendinger discloses or suggests the claimed step of "writing said image data directly into said AGP memory block of said system memory instead of said non-AGP memory block," claims 1-8 would not have been obvious from the combined disclosure of these patents.

Claims 9-17 recite that the received data is written into a specified memory block of said system memory, which is accessible by said graphics accelerator, without transference of the image data inside the system memory. As stated in the Office Action, this limitation is similar in scope to claims 1-8. For the reasons recited above, Applicants submit that claims 9-17 would not have been obvious from the combined disclosures of Datar, Miller, Ellenby, and Dendinger.

In view of the foregoing, Applicants respectfully request withdrawal of the rejections under Section 103(a) based upon the combined disclosures of Datar or Miller and Ellenby or Dendinger. Based on the above remarks, allowance of all pending claims 1-17 is respectfully requested. If there are any remaining issues preventing allowance of the pending claims that may be clarified by telephone, the Examiner is requested to call the undersigned.

Respectfully submitted,



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